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Performance Evaluation of Topologies Using NS-2

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ABSTRACT— A new chip design paradigm Network on Chip (NoC), proposed by many research groups is an important architectural choice for future System on Chips (SoCs). Various proposed NoC architecture attempts to address different component level architectures with specific interconnection network topologies and routing techniques. For NoC-based systems, performance could be modeled at different levels of abstraction. In the same context, improving systems performance could be achieved at different design phases. The interconnections among multiple cores on a chip have a significant impact on communication and performance of the chip design in terms of end-to-end delay, throughput, and packets loss ratio. Therefore, it is worthwhile studying the different characteristics of different topologies. Network Simulator (NS) is a name for series of discrete event network simulators, specifically; NS-1, NS-2 and NS-3. These simulators are used in the simulation of routing protocols, among others, and are heavily used in ad-hoc networking research, and support popular network protocols, offering simulation results for wired and wireless networks. NS-2 is primarily UNIX based and it uses Tool Command Language (TCL) as its scripting language.

I. INTRODUCTION

Over the past 40 years, the semiconductor industry has delivered continuous improvements in transistor density, approximately doubling the number of devices integrated on a die in every technology generation. As a result, starting with the Intel 4004 single chip CPU introduced in 1971 with 2300 transistors, on die device counts have grown by six orders of magnitude to over 2.3 billion in 2010 Intel Xeon Nehalem-EX.For much of this time, increasing transistor budgets were largely aimed at boosting single-threaded performance, which improved by as much as 50- 60% per year through the 1990's. Performance gains were derived through a combination of increased micro-architectural complexity and higher clock rates. In the early 2000's, however, a combination of factors that include design complexity considerations, growing wire delays, and power limitations of densely-integrated chips started limiting gains in core-level performance. Since then, core complexity has remained relatively constant, clock rates have stagnated, and growing transistor budgets have been devoted to additional cores, memories, and other on-chip resources.

Today, chip-level multiprocessors (CMPs) and systems on chip (SOC) are commonly found in a broad range of applications. These devices commonly integrate a combination of general-purpose cores, specialized hardware accelerator engines, caches, software-controlled memories, DRAM controllers, and I/O interfaces. Contemporary examples of such chips include a 16-core server processor from Sun/Oracle, an 80-core research prototype from Intel, and a 100-core processor from Tilera. Trends point in the direction of further integration, and chips containing thousands of cores and other resources are anticipated in the future.In a network, the topology is the arrangement of

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nodes and channels. It determines the interconnection of nodes and can usually be modeled as a graph. A topology has parameters such as degree, diameter, link complexity and bisection width, etc. These parameters together characterize a topology and distinguish one from the others. NS (network simulator) is a name for series of discrete event network simulators, specifically NS-1, NS-2 and NS-3. These simulators are used in the simulation of routing protocols, among others, and are heavily used in ad-hoc networking research, and support popular network protocols, offering simulation results for wired and wireless networks. It work at packet level & provide substantial support to simulate bunch of protocols like Transmission Control Protocol (TCP), User Datagram Protocol (UDP),File Transfer Protocol (FTP), Hypertext Transfer Protocol (HTTP) and Dynamic Source Routing (DSR). The NS-2 is a standard experiment environment in research community. Therefore NS-2 is used in this work.

II. NETWORK-ON-CHIP (NOC)

The 2D-mesh is the most common topology for NoCs in the open literature. It is also the common solution for the latest commercial proposals and industrial prototypes, like the Tilera multi-core processor family or the Intel 80 cores Polatis chip. However, this trend is expected to change in the near future due to the 2D-mesh limitations. Alterative topologies are either optimizations or modifications of a 2Dmesh. The topological structure of any interconnection network can be represented by a graph. Then, using graph theory concepts, we can analyze the performance of the interconnection network from different perspectives. Figure 1 shows eleven standard NoC topologies. This section presents some of the most promising regular topologies that have been recently proposed for NoCs in the open literature.

Eleven standard NoC topologies are –(a) Mesh (b) Torus (c) Folded Torus (d) Ring (e) Octagon (Oct) (f) Spidergon (Spider) (g) Binary tree (BT) (h) Butterfly Fat Tree (BFT) (i) SPIN (Scalable, Programmable, Integrated Network) (j) Hypercube (Hcube) (k) Star.

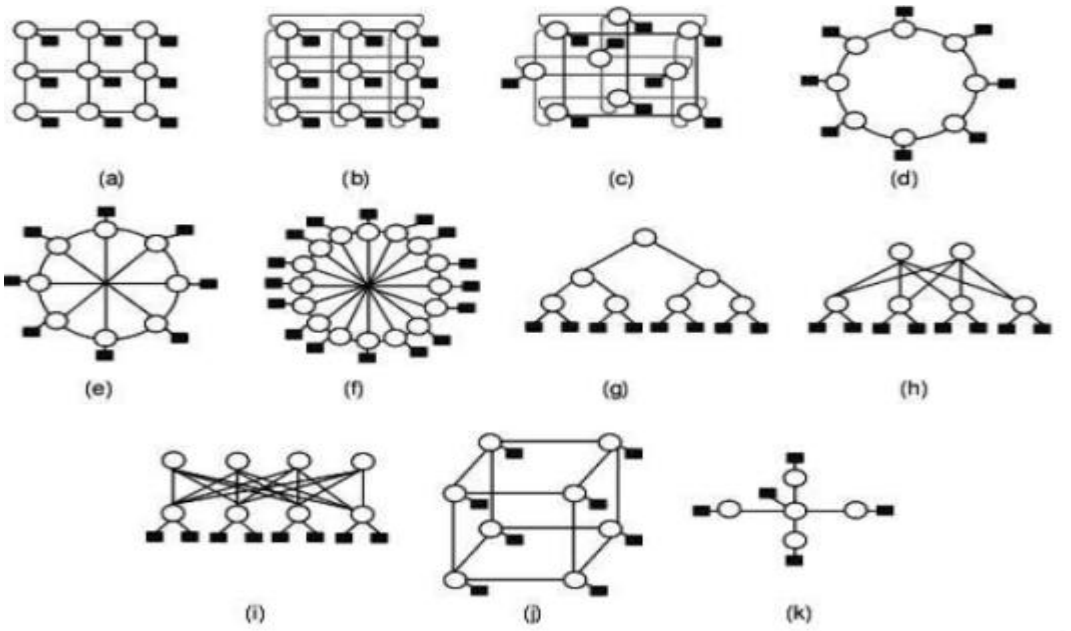

Fig 1. Eleven Standard NoC Topologies

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III. OVERVIEW OF NS-2

NS-2 went through from the NS version 1.0 was developed by the Network Research Group at the Lawrence Berkeley National Laboratory (LBNL) to the NS version 2 under which now part of the VINT project is. The VINT project is part of the University of Souther California. It unied the efforts of all people working in the field of network simulation, involving in MIT's NETSIM, University of Maryland's MARS, UC Berkeley's REAL, Columbia's NEST and LBNL's NS. At present, available network simulators rarely provide tools for visualization. However, for NS-2, it provides a NAM (Network ANimator, an animation tool for viewing the simulations results and packet trace data visually).

A good network simulator should be an effective tools for dissipating information about protocols. It should have a visual medium to make it easier to understand the working of a protocol. The ease of use and extensive features of one simulator will help the users in visualizing precisely, both the features and the working of the protocol in a constantly changing networking scenario.

NS is written in C++ and OTcl (is Tcl script language with Object oriented extensions developed at MIT). Tcl stands for Tool Command Language. Tcl is really two things: a scripting language, and an interpreter for that language that is designed to be easy to embed into your application. Tcl can provide a integration platform, and it can be a "glue" that assembles software building blocks into applications. In the architecture view of NS-2, a general user just design and run simulations in Tcl using the simulator objects in the OTcl library. The event schedulers and most of the network components are implemented in C++ and available to OTcl through an OTcl linkage that is implemented using tclcl.

IV. SYSTEM DEVELOPMENT

Because of very convenient commands and syntax of NS-2 for constructing network topology, it's easy to construct my 2-dimension mesh topology. The followings are some implementations of general commands for constructing topology. It's noticed that when the parameter appears first time in program, it's written without $. When it's called later, one prefix of "$" is necessitated. A pair of " " represents a value of this variable should be assigned or called here. Here the characteristics of 2D mesh, symmetric and uniform distribution, is took to construct it. On the base of syntax represented above, first step is to create a instance procedure to construct nodes and access operates.

Syntax:

- # Create a simulator object
- set /instance_name/ [new Simulator]
- # Create node
- set /node_name1/ [$instance_name node]
- set /node_name2/ [$instance_name node]
- # Create links between the nodes with Drop tail queue management mechanism $instance_name duplex-link $node_name1 $node_name2 /maximal_bandwidth/ /linkDelay/DropTail

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- # Set buffer size
- $instance_name queue-limit $node_name1 $node_name2 /buffSize/
- # Give node position (for NAM) $instance_name duplex-link-op $node_name1 $node_name2 orient /node_position/ Second step(line1 ~ line6) is to create the nodes of routers and resources.

The parameters, such as max bandwidth, link Delay, buffer Size, n x n and x, are necessarily required for constructing. nn determines the scale of topology. As mentioned before, a middle scale 4 X 4, was constructed, namely, x equals 4. max bandwidth represents the total maximum capacity of a network connection in the unit of Mbits s. link Delay means how long it will take to transfer a packet from one node to another on one link. It represents the time requirement for a packet to traverse a link. Both max bandwidth and linkDelay restrain the maximal network speed. The two parameters are given in default values, 200 Mbits s and 0.1 ms, respectively in NOC-S. buffer Size is a sensitive variable for many interesting results of being expected. Three topologies are developed in this work namely; mesh, custom1 and custom2 topology.

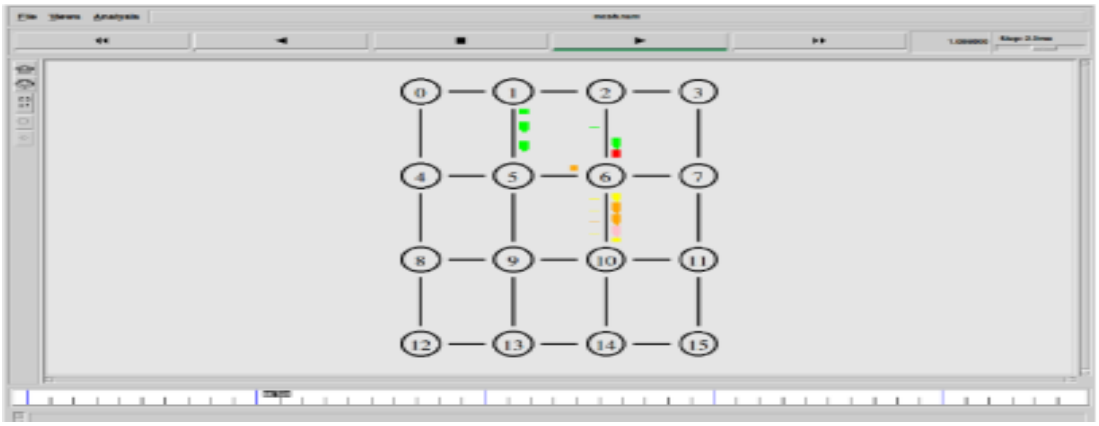

Fig 2. Screenshot of Mesh Topology

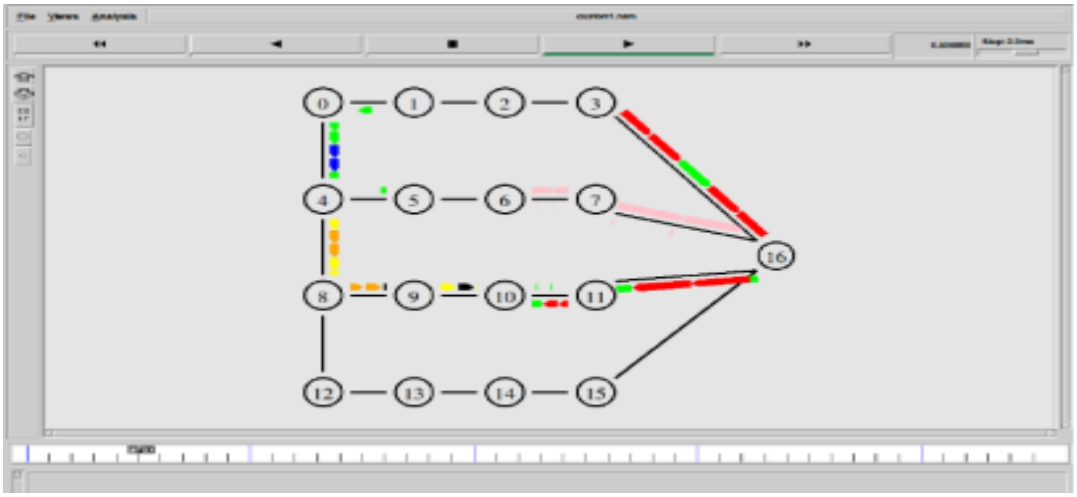

Fig 3. Screenshot of Custom1 Topology

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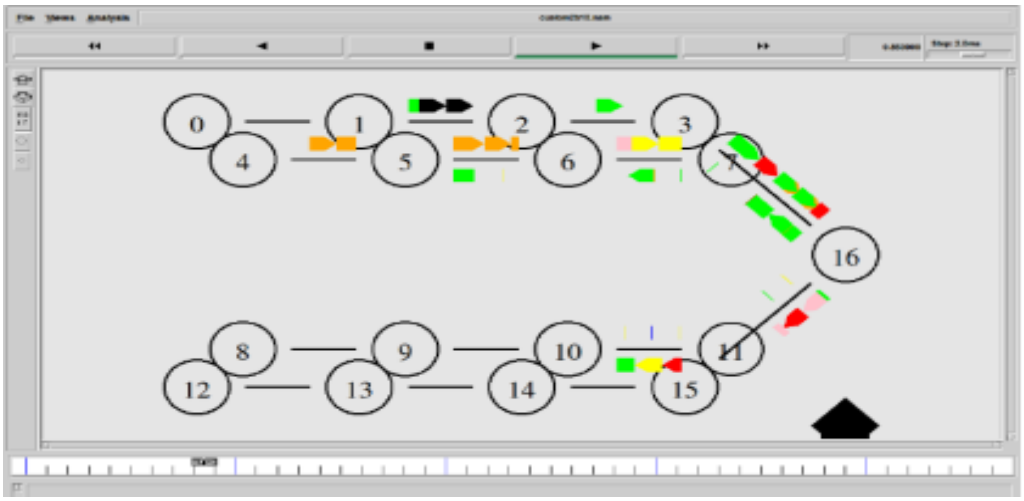

Fig 4. Screenshot of Custom2 Topology

V. PERFORMANCE ANALYSIS

Based on the results obtained and various graphs plotted, the performance of all the three topologies can be evaluated. Table-1 gives the performance evaluation of mesh, custom1 and custom2 topology.

Table-1: Performance Evaluation of Various Topologies

Parameter	Mesh Topology	Custom1 Topology	Custom1 Topology
Throughput	Medium (Max 750)	Highest (Max 1020)	Lowest (Max 605)
End2End Delay	Max 0.08 sec.	Max 0.12 sec.	Max 0.15 sec.
Jitter	Avg. 0.15 sec.	Avg. 0.17 sec.	Avg. 0.18 sec.
Dropped Packets	7	3	6

From Table-1 it is seen that, throughput is maximum and packet loss is minimum in case of custom1 topology. However, in this case jitter is much more than mesh topology. These results indicate that, the in stead of using regular topologies; some sort custom topologies must be be tried for NoC. So that, the performance of NoC will be improved.

However, the problem with the implementation of new and custom topology is that; there is a lack of information about many other and conventional characteristics of the topology. This can be the demerit for computer networks but for NoC the new and custom topology is practically implemented only when it is proved satisfactory for computer networks.

Therefore, new or custom topologies must be first tried on computer networks and after successful implementation they must be tried for NoC. NoC is very dedicated and crucial application of computer networks technology. Also, NoC is one unit implementing the targeted and programmed things. Therefore, almost care must be taken while implementing new or custom topology for NoC.

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The research work carried out in this paper shows that, custom1 topology is the best for NoC and it should be implemented in all future NoC systems. However, regarding the performance parameters detail study must be carried out in terms of theoretical and practical work before the implementation of the topology. This is because, all the conventional and practical topologies are the result of thorough and deep study of the many researchers.

VI. CONCLUSION

NoCs have tackled the SoCs disadvantages. Mesh, custom1 and custom2 are the three NoC topologies presented in this dissertation. Finally the comparisons of mesh, custom1 and custom2 topologies carried out for different figures of merit such as throughput, end2end delay, jitter and dropped packets, etc, Custom1 always has better performance parameters than mesh and custom2. However the cost we pay for this improvement is higher jitter. The experiment proved that the more adaptiveness a routing algorithm has, the lower power consumption in the custom1 topology is. So the XY routing as a deterministic routing is not a suitable routing algorithm for custom1 topology. Routing algorithms, traffic models and number of virtual channels have a direct effect on power consumption and give rise to interesting trade-offs. It is proved that adaptive routing algorithms effectively utilize the wrap-around links in custom1 topology.

The following series of simulation results were obtained:

- Throughput is maximum in case of custom1 topology. This is really very good sign.
- End2end delay is minimum in case on mesh topology.
- The effect of buffer size is least in case of custom1 topology and respectively more in case of mesh and custom2 topology.
- The drop possibility is more sensitive on communication load than buffer size in the range of small buffer size.
- Jitter is minimum in case of mesh topology.
- However, packet loss is maximum in case of mesh topology (= 7), medium in case of custom2 topology (= 6) and minimum in case of custom1 topology (= 3).

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