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Performance Evaluation of Network on Chip Architectures Using Network Simulator-2

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ABSTRACT— A new chip design paradigm Network on Chip (NoC), proposed by many research groups is an important architectural choice for future System on Chips (SoCs). Various proposed NoC architecture attempts to address different component level architectures with specific interconnection network topologies and routing techniques. For NoC-based systems, performance could be modeled at different levels of abstraction. In the same context, improving systems performance could be achieved at different design phases. The interconnections among multiple cores on a chip have a significant impact on communication and performance of the chip design in terms of end-to-end delay, throughput, and packets loss ratio. Therefore, it is worthwhile studying the different characteristics of different topologies. Network Simulator (NS) is a name for series of discrete event network simulators, specifically; NS-1, NS-2 and NS-3. These simulators are used in the simulation of routing protocols, among others, and are heavily used in ad-hoc networking research, and support popular network protocols, offering simulation results for wired and wireless networks. NS-2 is primarily UNIX based and it uses Tool Command Language (TCL) as its scripting language.

I. INTRODUCTION

To meet the growing computation-intensive applications and the needs of low-power, high-performance systems, the number of computing resources in single-chip has enormously increased, because current VLSI technology can support such an extensive integration of transistors. By adding many computing resources such as CPU, DSP, specific IPs, etc to build a system in System-on-Chip, its interconnection between each other becomes another challenging issue. In most System-on-Chip applications, a shared bus interconnection which needs arbitration logic to serialize several bus access requests, is adopted to communicate with each integrated processing unit because of its low-cost and simple control characteristics.

Network-on-Chip (NoC) is an approach to designing the communication subsystem between IP cores in a System-on-a-Chip (SoC). NoCs can span synchronous and asynchronous clock domains or use unclocked asynchronous logic. NoC applies networking theory and methods to on-chip communication and brings notable improvements over conventional bus and crossbar interconnections. NoC improves the scalability of SoCs, and the power efficiency of complex SoCs compared to other designs. Network-on-Chip (NoC) is an emerging paradigm for communications within large VLSI systems implemented on a single silicon chip.

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NS-2 is a discrete event simulator targeted at networking research. Ns provides substantial support for simulation of TCP, routing, and multicast protocols over wired and wireless (local and satellite) networks.

II. NETWORK-ON-CHIP (NOC)

Such scalable bandwidth requirement can be satisfied by using on-chip packet-switched micro-network of interconnects, generally known as Network-on-Chip (NoC) architecture. The basic idea came from traditional large-scale multi-processors and distributed computing networks. The scalable and modular nature of NoCs and their support for efficient on-chip communication lead to NoC-based system implementations. Even though the current network technologies are well developed and their supporting features are excellent, their complicated configurations and implementation complexity make it hard to be adopted as an on-chip interconnection methodology. In order to meet typical SoCs or multi-core processing environment, basic module of network interconnection like switching logic, routing algorithm and its packet definition should be light-weighted to result in easily implemental solutions [1].

In communication between several cores in System-on-Chip (SoC) environment, some prevailing mechanisms for this purpose are several bus-based architectures and point-to-point communication methodologies. For simplicity and ease of use, the bus-based architectures are the most common. However, in bus-based architecture, it has fundamentally some limitation in bandwidth. To overcome such a limitation of communication and overcome such an enormous wiring delay in future technology is to adopt network-like interconnections which are called Network-on-Chip (NoC) architecture. Replacement of SoC busses by NoCs will follow the same path of data communications when the economics prove that the NoC either reduces SoC manufacturing cost, SoC time to market, and SoC design risk or increases SoC performance [1].

Traditionally, ICs have been designed with dedicated point-to-point connections, with one wire dedicated to each signal. For large designs, in particular, this has several limitations from a physical design viewpoint. The wires occupy much of the area of the chip, and in nanometer CMOS technology, interconnects dominate both performance and dynamic power dissipation, as signal propagation in wires across the chip requires multiple clock cycles [2].

NoC links can reduce the complexity of designing wires for predictable speed, power, noise, reliability, etc., thanks to their regular, well controlled structure. From a system design viewpoint, with the advent of multi-core processor systems, a network is a natural architectural choice. A NoC can provide separation between computation and communication; support modularity and IP reuse via standard interfaces, handle synchronization issues, serve as a platform for system test, and, hence, increase engineering productivity [2].

In designing NoC systems, there are several issues to be concerned with, such as topologies, routing algorithms, performance, latency, complexity and so on. Among these factors, nothing can be independent in deciding an NoC architecture. There are several different kinds of topologies [2].

III. NETWORK SIMULATOR (NS)

NS is a discrete event simulator targeted at networking research. NS provides substantial support for simulation of TCP, routing, and multicast protocols over wired and wireless networks [3].

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NS began as a variant of the REAL network simulator in 1989 and has evolved substantially over the past few years. In 1995 ns development was supported by DARPA through the VINT project at LBL, Xerox PARC, UCB, and USC/ISI. Currently ns development is support through DARPA with SAMAN and through NSF with CONSER, both in collaboration with other researchers including ACIRI [4].

3.1. Version History

1. NS-1: The first version of NS, known as NS-1, was developed at Lawrence Berkeley National Laboratory (LBNL) in the 1995-97 timeframe by Steve McCanne, Sally Floyd, Kevin Fall, and other contributors. This was known as the LBNL Network Simulator, and derived from an earlier simulator known as REAL by S. Keshav. The core of the simulator was written in C++, with Tcl-based scripting of simulation scenarios. Long-running contributions have also come from Sun Microsystems, the UC Berkeley Daedelus, and Carnegie Mellon Monarch projects [5].

2. NS-2: In 1996-97, work on NS version 2 (NS-2) was initiated based on a refactoring by Steve McCanne. Use of Tcl was replaced by MIT's Object Tcl (OTcl), an object-oriented dialect of Tcl. The core of NS-2 is also written in C++, but the C++ simulation objects are linked to shadow objects in OTcl and variables can be linked between both language realms. Simulation scripts are written in the OTcl language, an extension of the Tcl scripting language. In the timeframe in which NS-2 was introduced (mid-1990s), this provided both a significant convenience in avoiding many time-consuming recompilations, and also allowing potentially easier scripting syntax for describing simulations [5].

Presently, NS-2 consists of over 300,000 lines of source code, and there is probably a comparable amount of contributed code that is not integrated directly into the main distribution (many forks of NS-2 exist, both maintained and unmaintained). It runs on GNU/Linux, FreeBSD, Solaris, Mac OS X and Windows 95/98/NT/2000/XP. It is licensed for use under version 2 of the GNU General Public License [5].

3. NS-3: Work on NS-3 began in the 2004-05 timeframe. A team led by Tom Henderson (University of Washington), and also including George Riley (Georgia Tech), Sally Floyd (International Computer Science Institute), and Sumit Roy (University of Washington), applied for and received funding from the U.S. National Science Foundation (NSF) to build a replacement for NS-2, called NS-3. Around the same time, the Planete research team at INRIA Sophia Antipolis, including principally Mathieu Lacage and Walid Dabbous, began to explore a replacement for NS-2, with an initial emphasis on IEEE 802.11 Wi-Fi models. Lacage's initial simulator was named Yet Another Network Simulator (YANS) [5].

3.2. Simulation Workflow

The general process of creating a simulation can be divided into several steps [6]:

(i) Topology definition, (ii) Model usage, (iii) Node and link configuration, (iv) Execution, (v) Performance analysis, and (vi) Graphical Visualization. Figure 1 shows the simplified user view of NS-2.

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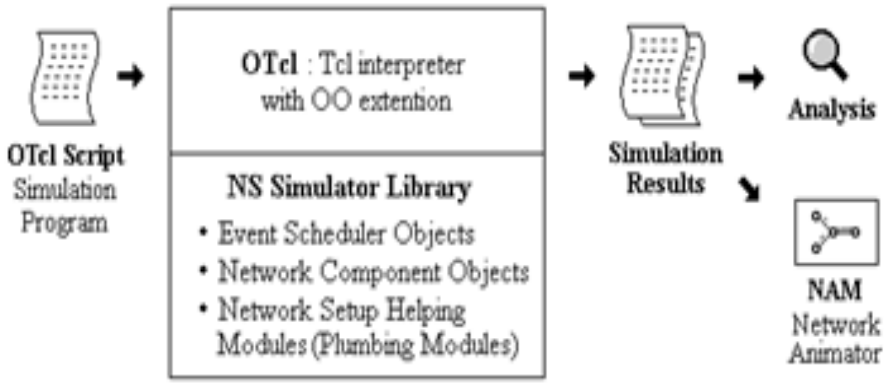

Fig 1. Simplified User's View of NS

IV. SYSTEM DEVELOPMENT

The NoC simulation model (NoC-S) is mainly composed of four parts, topology, traffic scenario generator, simulation control, and recorder monitor, as shown in Figure 2. All of them satisfy the communication requirement of NoC. In this model, only is the NoC region using CLICHE approach with heterogeneous resources mapped, simulated and analyzed [7].

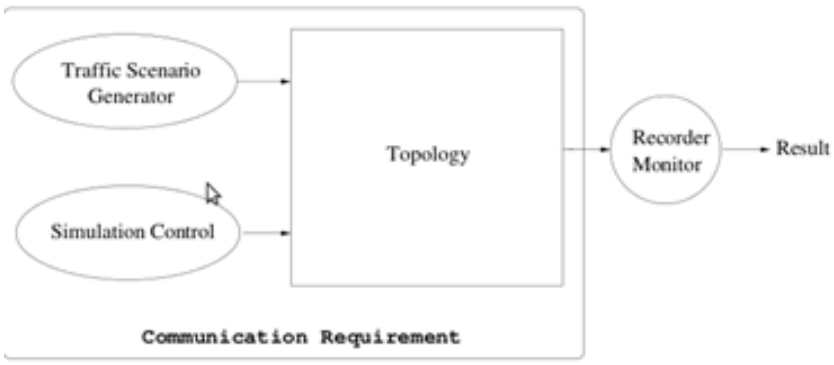

Fig 2. NoC Simulator Model

V. RESULTS FOR MESH TOPOLOGY

The mesh topology simulation results are obtained. Following Figure 3 shows screenshot of 3x3 mesh where, nn=9. In this Figure 3 square and circle represent router and resources.

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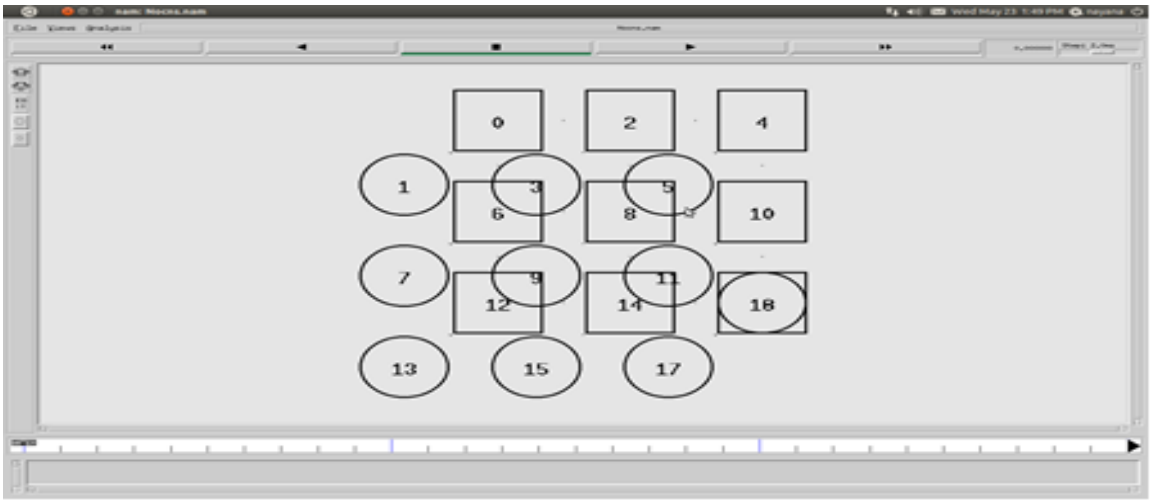

Fig 3. Screenshot of 3x3 Mesh

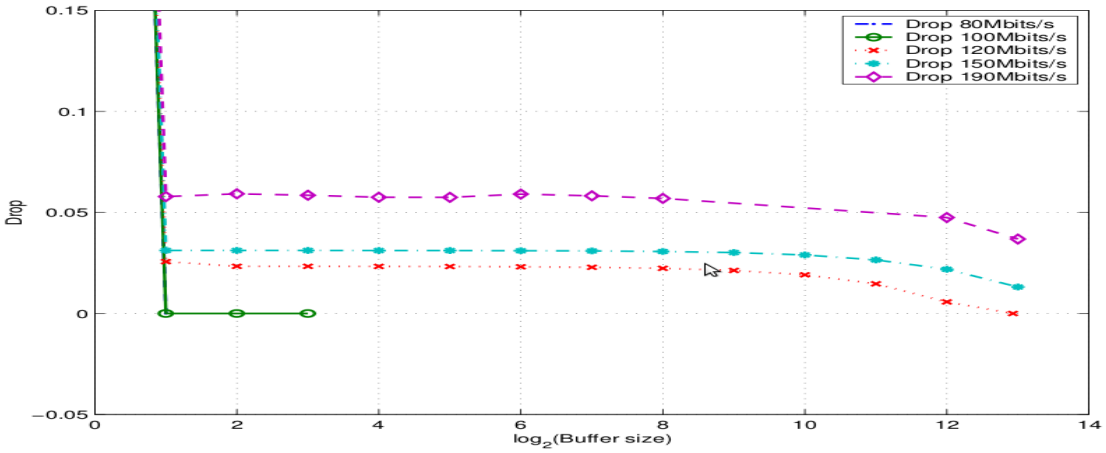

Fig 4. Drop Possibility vs. Buffer Size

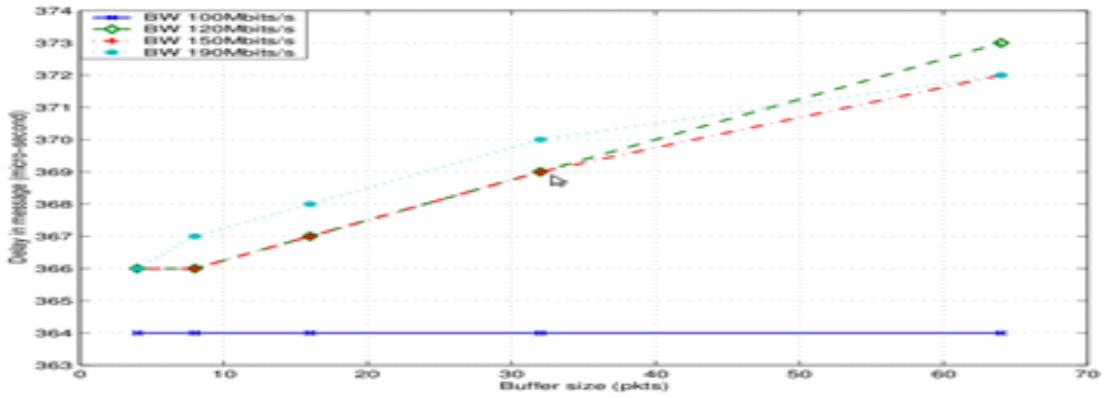

Fig 5. Buffer Utilization vs. Buffer Size

Figure 4 shows Drop Possibility vs. Buffer Size and Figure 5 shows Buffer Utilization vs. Buffer Size for 3x3 mesh topology.

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VI. CONCLUSION

Following conclusions are drawn based on the results obtained for 3x3 mesh topology –

- Increasing buffer size does not make an obvious advantage for decreasing the number of drop packets.
- The drop possibility is more sensitive on communication load than buffer size in the range of small buffer size.
- The reasonable Mbuffer size is around 4 pkts or 8 pkts.
- Delay in queue is important part for delay in message.

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