Dynamic Power Saving For Multiplier

Mr. Rahul Pimpale[1], Prof. S.P.Patil[2]

PG Scholar, Dept. of E&TC Engg.,PSGVP Mandal D.N.Patel College of Engg.,Shahada,M.S.,India[1]
Associate Professor, Dept. of E&TC Engg.,PSGVP Mandal D.N.Patel College of Engg.,Shahada,M.S.,India[2]

*ABSTRACT-*This paper is related to development of a multiprecision (MP) reconfigurable multiplier with dynamic voltage scaling. All of the building blocks of the proposed reconfigurable multiplier can either work as independent smaller-precision multipliers or work in parallel to perform higher-precision multiplications. Given the user's requirements a dynamic voltage/frequency scaling management unit configures the multiplier to operate at the proper precision and frequency. Adapting to the run-time workload of the targeted application, razor flip-flops together with a dithering voltage unit then configure the multiplier to achieve the lowest power consumption. Adapting to the run-time workload of the targeted application, razor flip-flops combine with a dithering voltage unit, because of this the multiplier is able to achieve the lowest power consumption. Use of single switch dithering voltage unit and razor flip-flops help to minimize the safety margins in voltage and overhead in DVS.

KEYWORDS- **M**ultiprecision (MP), Multiplier with dynamic voltage scaling, razor flip-flops, DVS.

I. INTRODUCTION

Today, 'energy crises' is the main problem facedby the worldwide technologies. So, the main aim is reduction in power consumption of circuit to avoid the energy crises problem.Consumers demand for increasingly portable yet high performance multimedia and communication products imposes stringent constraints on the power consumption of individual internal components. Of these, multipliers perform one of the most frequently encountered arithmetic operations in digital signal processors (DSPs). For embedded applications, it has become essential to design more power-aware multipliers. Given their fairly complex structure and interconnections, multipliers can exhibit a large number of unbalanced paths, resulting in substantial glitch generation and propagation. This spurious switching activity can be mitigated by balancing internal paths through a combination of architectural and transistor-level optimization techniques.

In addition to equalizing internal path delays, dynamic power reduction can also be achieved by monitoring the effective dynamic range of the input operands so as to disable unused sections of the multiplier and/or truncate the output product at the cost of reduced precision . This is possible because, in most sensor applications, the actual inputs do not always occupy the entire magnitude of its word-length. For example, in artificial neural network applications, the weight precision used during the learning phase is approximately twice that of the retrieval phase. In contrast, most of today's full-custom DSPs and application-specific integrated circuits (ASICs) are designed for a fixed maximum word-length so as to accommodate the worst case scenario. Therefore, an 8-bit multiplication computed on a 32-bit Booth multiplier would result in unnecessary switching activity and power loss.

In Most applications are based on 8–16-b operand, the proposed multiplier is designed to not only perform single 16-bit but also performs single 8-bit, or twin parallel 8-bit multiplication operations. in some applications,16

and 32 bit operands are send to smaller multiplication circuit with parallel operation reduce power consumption and also reduces area over head. Due to the complex structure and interconnections, multipliers have large amount of unbalanced path which causes unwanted signal generation and propagation. This can be avoided by proper internal balancing through architectural and transistor level optimization. In most cases of multipliers, maximum word length is provided. Hence small multiplications are done in large multipliers, this causes unwanted switching activity and also power consumption. So word length optimization is the best method in which 8-bit multiplier is reused for 16-bit and 32-bit multiplication. Here it is possible to incorporate the pipelining for increasing the speed of the multiplier.

II.   LITERATURE REVIEW

Several works investigated this word-length optimization. Proposed an ensemble of multipliers of different precisions, with each optimized to cater for a particular scenario. Each pair of incoming operands is routed to the smallest multiplier that can compute the result to take advantage of the lower energy consumption of the smaller circuit. This ensemble of point systems is reported to consume the least power but this came at the cost of increased chip area given the used ensemble structure. To address this issue proposed to share and reuse some functional modules within the ensemble. In an 8-bit multiplier is reused for the16-bit multiplication, adding scalability without large area penalty. This method is extended by implementing pipelining to further improve the multiplier's performance. A more flexible approach is proposed in , with several multiplier elements grouped together to provide higher precisions and re configurability. This analysis showed that around 10%–20% of extra chip area is needed for 8–16 bits multipliers.

III.   MULTIPLIER SYSTEM

The proposed MP multiplier system (Fig.1) consist five different components that are as follows:

1) MP multiplier;

2) Input Operands Scheduler (IOS)

3) Frequency Scaling Unit

4) Voltage Scaling Unit (VSU)
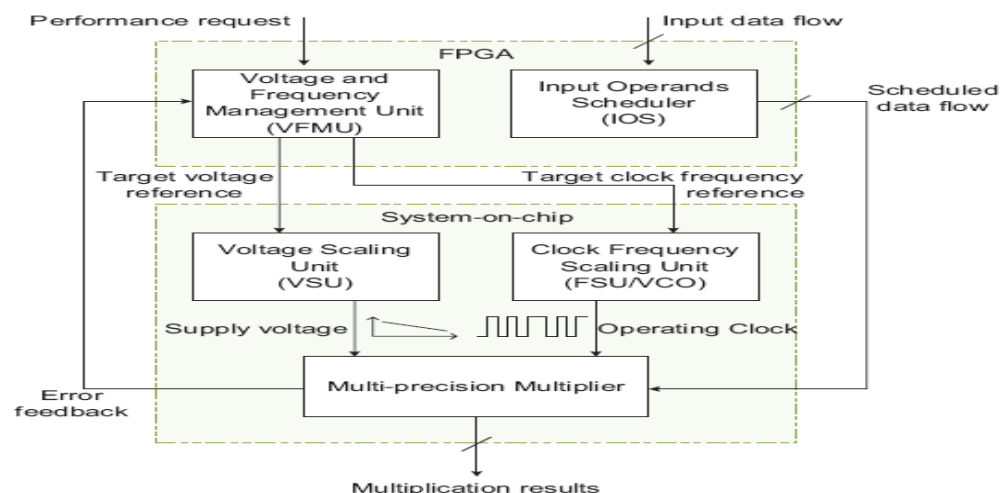
5)Dynamic Voltage/Frequency Management Unit (VFMU)

Fig. 1 Multiplier system

1) **IOS (Input operand scheduler):**

The input operands scheduler which rearranges the input data and hence reduce the supply voltage transition, thus power consumption will be reduced. It consists of range detector, buffer (RAM), and a voltage and frequency analyzer. These help to rearrange the input and detect the precision and send to MP multiplier.IOS that will perform the following tasks:

Reorder the input data stream so that same-precision operands are grouped together into a buffer and take the minimum supply and frequency from the LUT.

2) **Frequency Scaling Unit**

Frequency scaling unit of proposed MP multiplier is used for frequency tuning to meet the system throughput requirements. The frequency scaling unit is one which equipped with VCO is used to select frequency for each combination of multiplication. Depending on the control signal, it gives frequency that pre-calculated for 8 x 8bit, 16 x 16 bit and 32 x 32 bit for proper multiplication to reduce delay. Depending on the voltage VCO adjust the frequency. For each combination of multiplication, we can select the corresponding suitable frequency.

3) **Voltage Scaling Unit**

The voltage scaling unit (VSU) , its function is to dynamically generate the supply voltage so as to minimize power consumption.

4) **Voltage /frequency management unit:**The dynamic voltage/frequency management unit (VFMU) that receives the user requirements (e.g. throughput).The VFMU sends control signals to the VSU and FSU to generate the required power supply voltage and clock frequency for the MP multiplier.

5) **Dynamic Voltage Scaling:**The system can operate at different voltage supply according to the workload that's why we use dynamic voltage scaling. Dynamic voltage scaling reduces the power consumption.

Timing/Voltage Values: DVFS uses a set of discrete voltage or frequency pairs. Determining which values to support is a key design decision and application dependent.

The Effects of Temperature Inversion: Voltages must be limited to the range over which delay and voltage track that either never decreases or never increases as its independent variable increases, which means above the temperature inversion point. Below the temperature inversion point, delay and voltage invert their normal relationship.

Libraries: To establish what voltage levels are needed for the selected clock frequency, we need do trial implementation at reduced voltages and measure the performance. Therefore we need libraries whose characterization extends beyond their nominal supply voltages.

Switching Times and Algorithms: Switching performance levels take time for both voltage regulators and clock generators. Switching voltage levels is particular slow and switching frequencies is orders of magnitude faster than voltage level switching. Increase the voltage first and decrease the voltage after the frequency is lowered.

LUT: LUT-based FPGAs are used already for implementing digital designs in a wide variety of application domains. LUTs are used for reducing delay, area, and power consumption, improving rout ability and resource utilization, and increasing expressive power of programmable logic. Reducing delay is especially important as it allows high-frequency FPGAs. Delay in modern FPGAs is dominated by interconnect.
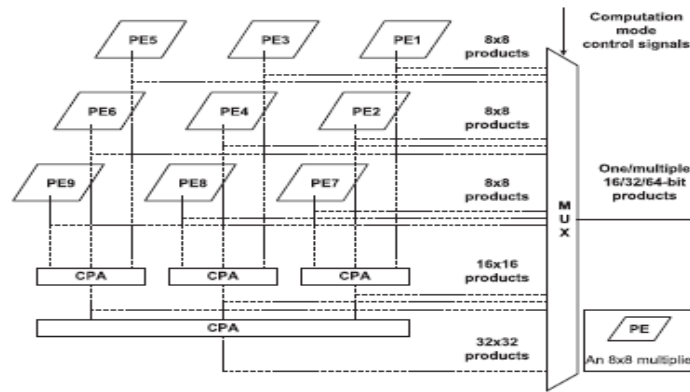
Fig. 2 Possible configuration modes of proposed MP multiplier.

Reversible Logic Gates:

For the multiplicationwe use reversible logic gates. For 4x4 vedic multiplier that optimized by reducing the number of logic gates and constant inputs and garbage outputs. Byusing reversible gates require less gates that reduces power requirement, less area and also less delay that is increases speed.

Kogge-Stone Adder:

Doing any multiplication we require adder for adding partial product term in multiplication. For adding partial product term we use kogge stone adder. by using Kogge stone adder it increases power performance of the multiplier. Kogge stone adder have lower fanout at each stage that increases performance.Variable latency adders have been recently proposed in literature. A variable latency adder employs speculation: the exact arithmetic function is replaced with an approximated one that is faster and gives the correct result most of the time, but not always.

The approximated adder is augmented with an error detection network that asserts an error signal when speculation fails. Speculative variable latency adders have attracted strong interest thanks to their capability to reduce average delay compared to traditional architectures. This paper proposes a novel variable latency speculative adder based on Han-Carlson parallel-prefix topology that resulted more effective than variable latency Kogge-Stone topology.Several variable latency speculative adders, for various operand lengths, using both Han-Carlson and Kogge-Stone topology.Obtained results show that proposed variable latency Han-Carlson adder outperforms both previously proposed speculative Kogge-Stone architectures and non-speculative adders, when high-speed is required. It is also shown that non-speculative adders remain the best choice when the speed constraint is relaxed.

Basic Adder Unit: A combinational circuit that adds two bits is called a half adder. A full adder is one that adds three bits, the third produced from a previous addition operation.
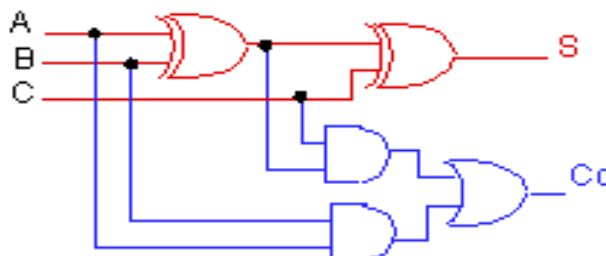

Fig. 3 Half Adder and Full Adder

Boolean equation

Sum=A xor B xorCin;

Carry=(A and B)or(A and Cin)or (B and Cin);

Its mean one full adder consist 7 gates is below 2 xor,3 and ,2 or gates.

Ripple Carry Adder

The ripple carry adder is constructed by cascading full adder blocks in series. The carryout of one stage is fed directly to the carry-in of the next stage. For an n-bit parallel adder, it requires n full adders.
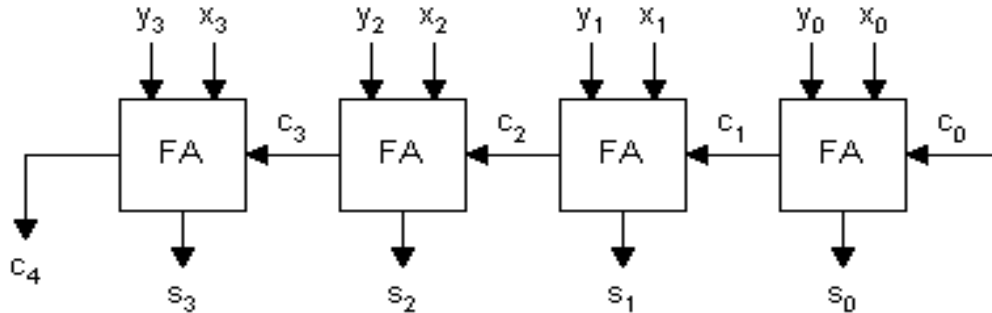

Fig. 4 Ripple Carry Adder

If we taken the 16 bit Ripple carry adder mean its consist of 16 full adder.One full adder consist of 7 gates mean16 bit Ripple carry adder consist of 16*7=112 gates.

Carry Look-Ahead Adder: Calculates the carry signals in advance, based on the input signals

Boolean Equations

$P_i = A_i \oplus B_i$Carry propagate

$G_i = A_i B_i$Carry generate

$S_i = P_i \oplus C_i$ Sum

$C_{i+1}= G_i + P_i C$Carry out

Signals P and G only depend on the input bits. If we taken 16 bit adder means it required 135 gates.
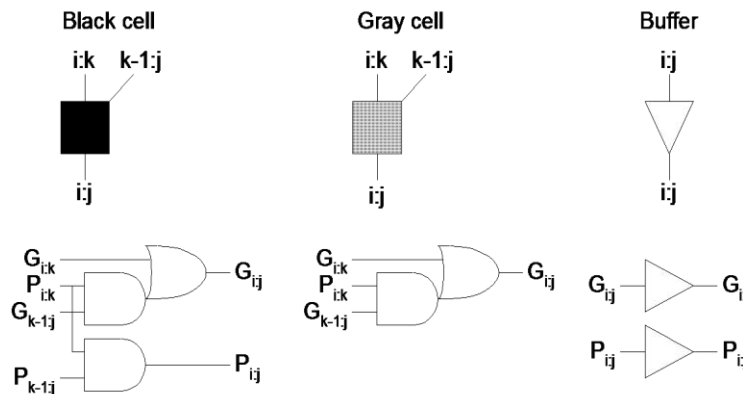

Fig. 5 Notations of Cell

Kogge-Stone Adder

One black cell consist of 3 gates is 2 and , one or gate.Kogge- stone adder consist of 33 black cell 35*3=105 gates is required .
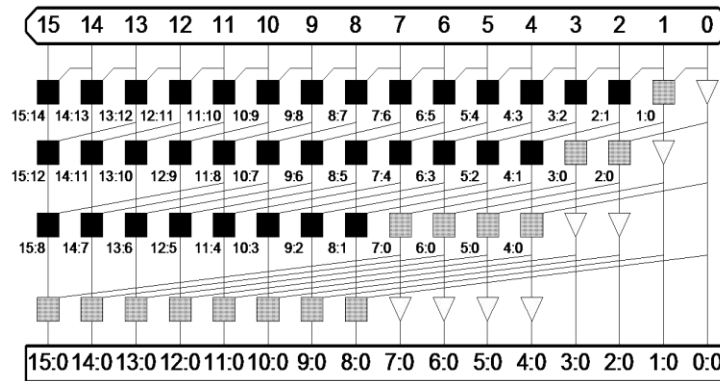
Fig. 6 Kogge stone Adder

Adder	Required gates
Ripple carry adder	112
Carry look ahead adder	135
Kogge stone adder	105

Table 1: Comparisons of Adders

System Flow:

The flow of system is shown in fig. In system flow first it scans the given input then by using select line it accepts multiplicand. It generates control signal. Control signal is passes to MP multiplier, frequency division scaling, voltage scaling and FPGA kit for relays operation. Multiplication result output display on LCD.
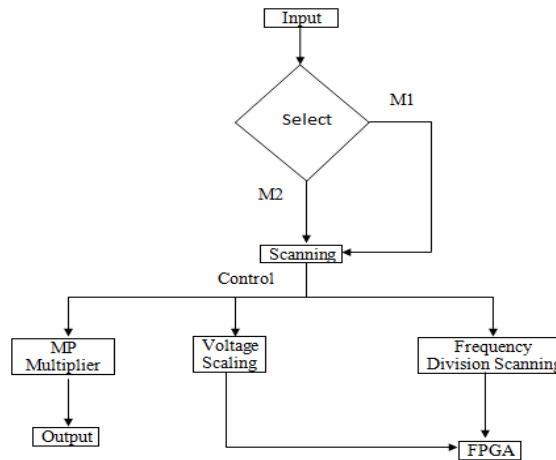

Fig. 7 System Flow

Flow of project

1) First we design the input scheduler. its check the input bit range and according to range its generate the control signal.

2) The control signal passes to the management unit and MP multiplier.

3) Management unit scale the voltage and frequency according to control signal .

4) Power supply 5v Voltage scale into 1.2V,2.2V,3.3V using voltage regulator.

5) The kit frequency 12MHz scale into the 6MHz,3MHz using frequency scaling method.

6) Multi precision multiplier consist of 8x8,16x16,32x32 multiplier

7) Processing element .According to the control signal its choose multiplier using the multiplexer .

8) Accordingto the input rang we get output.

9) In 8x8,16x16,32x32 multiplier using the RCA(Ripple Carry Adder) it has some drawback like required more gate ,delay , power .

10)If we replace the RCA(Ripple Carry Adder) by kogge stone adder. kogge stone adder required the less gate ,power ,delay as compare to the RCA(Ripple Carry Adder

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